BOX ISSUE FEE
PATENT

IN THE U.S. PATENT AND TRADEMARK OFFICE

Application No.:	10/761,239	Group Art Unit:	2816
Filing Date:	January 22, 2004	Examiner:	Terry Lee Englund
Applicant:	Jong-Hyun CHOI	Confirmation No.:	3822
Title:	SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE WITH DUAL INSULATION SYSTEM (AS AMENDED)		
Attorney Docket:	8947-000068/US		

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Randolph Building
401 Dulany Street
Alexandria, VA 22314
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May 11, 2009

COMMENTS ON THE EXAMINER'S
STATEMENT OF REASONS FOR ALLOWANCE

Sir:

In reply to the Examiner's Statement of Reasons for Allowance, provided with the Notice of Allowance dated May 11, 2009, Applicants submit the following comments.

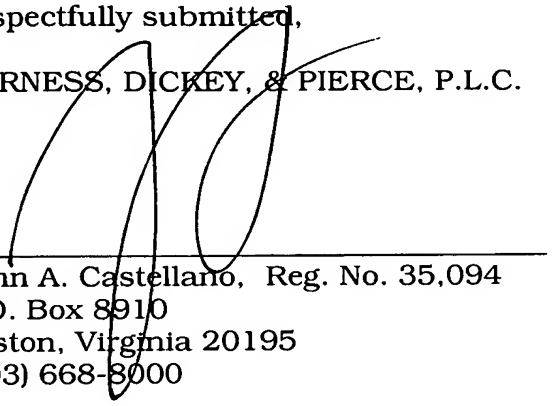
The Examiner offers several reasons why the claims of the present application are allowable over the prior art of record. Although Applicants agree that the various claimed limitations mentioned in the claims are not taught or suggested by the prior art taken either singly or in combination, Applicants wish to emphasize that it is each claim, taken as a whole, including the interrelationships and interconnections between various claimed elements which is allowable over the prior art of record.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano, Reg. No. 35,094 at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By 

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JAC/mth